74ABT125

Quad buffer; 3-state

Rev. 6 — 3 November 2011 Product data sheet

1. General description

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling one of the 3-state outputs.

2. Features and benefits

- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH –32 mA; LOW +64 mA
- Power-up 3-state
- Inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT125N	–40 °C to +85 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74ABT125D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT125DB	–40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74ABT125PW	–40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ABT125BQ	–40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

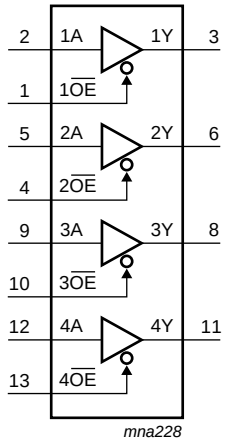


Fig 1. Logic symbol

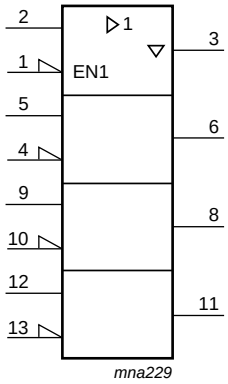


Fig 2. IEC logic symbol

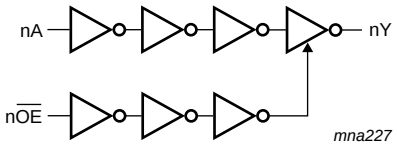


Fig 3. Logic diagram (one buffer)

5. Pinning information

5.1 Pinning

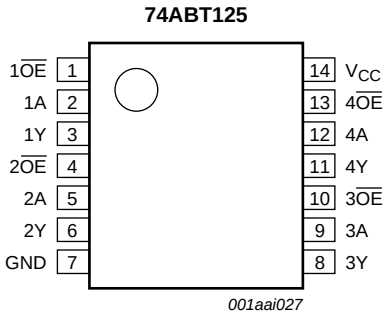
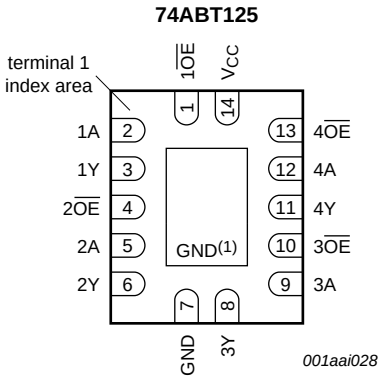


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$ to $4\overline{OE}$	1, 4, 10, 13	output enable input (active LOW)
1A to 4A	2, 5, 9, 12	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function selection[1]

Inputs		Output
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values[1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state		–0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] SO14 packages: above 70 °C P_{tot} derate linearly with 8 mW/K
SSOP14 and TSSOP20 packages: above 60 °C P_{tot} derate linearly with 5.5 mW/K
DHVQFN14 packages: above 60 °C P_{tot} derate linearly with 4.5 mW/K

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8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage		0	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level Input voltage		-	0.8	V
I_{OH}	HIGH-level output current		–32	-	mA
I_{OL}	LOW-level output current		-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	–0.9	–1.2	-	–1.2	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = –3 mA		2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA		3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; $V_I = V_{IL}$ or V_{IH}		-	0.35	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_I or $V_O \leq$ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{OE}$ = don't care	[1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; $V_I = V_{IL}$ or V_{IH}							
		V_O = 2.7 V		-	1.0	50	-	50	µA
		V_O = 0.5 V		-	–1.0	–50	-	–50	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–50	–100	–180	–50	–180	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	65	250	-	250	µA
		outputs LOW-state		-	12	15	-	30	mA
		outputs disabled		-	65	250	-	50	µA

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Table 6. Static characteristics *…continued*

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
ΔI_{CC}	additional supply current	per control pin; V_{CC} = 5.5 V; one control input at 3.4 V, other inputs at V_{CC} or GND [3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA
		outputs disabled	-	50	250	-	250	mA
		one enable input at 3.4 V and other inputs at V_{CC} or GND; outputs disabled	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}	-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

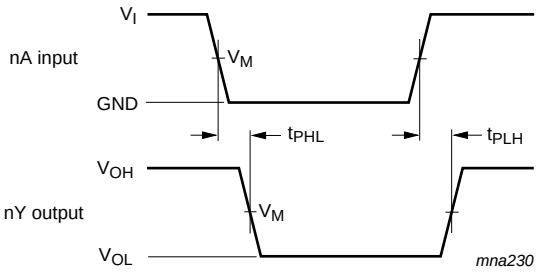
GND = 0 V. Test circuit is shown in Figure 8.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nA to nY, see Figure 6	1.0	2.8	4.1	1.0	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Figure 6	1.0	3.1	4.6	1.0	4.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nY; see Figure 7	1.0	3.2	5.0	1.0	5.9	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nY; see Figure 7	1.0	4.2	6.2	1.0	6.8	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nY; see Figure 7	1.0	4.1	5.4	1.0	6.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nY; see Figure 7	1.5	2.8	5.0	1.5	5.5	ns

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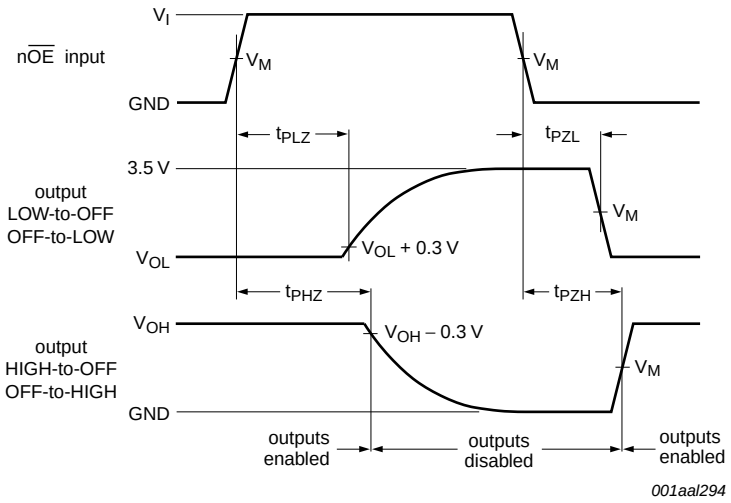
11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (nA) to output (nY)



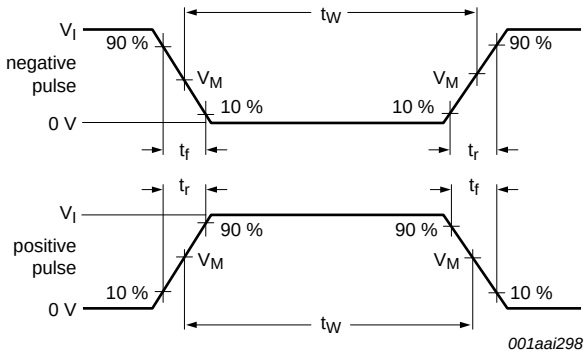
V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

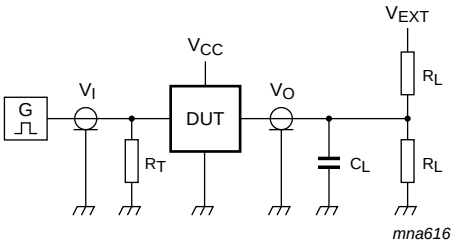
Fig 7. Enable and disable times

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a. Input pulse definition



b. Test circuit

Test data is given in Table 8.

Test circuit definitions:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 8. Load circuitry for switching times

Table 8. Test data

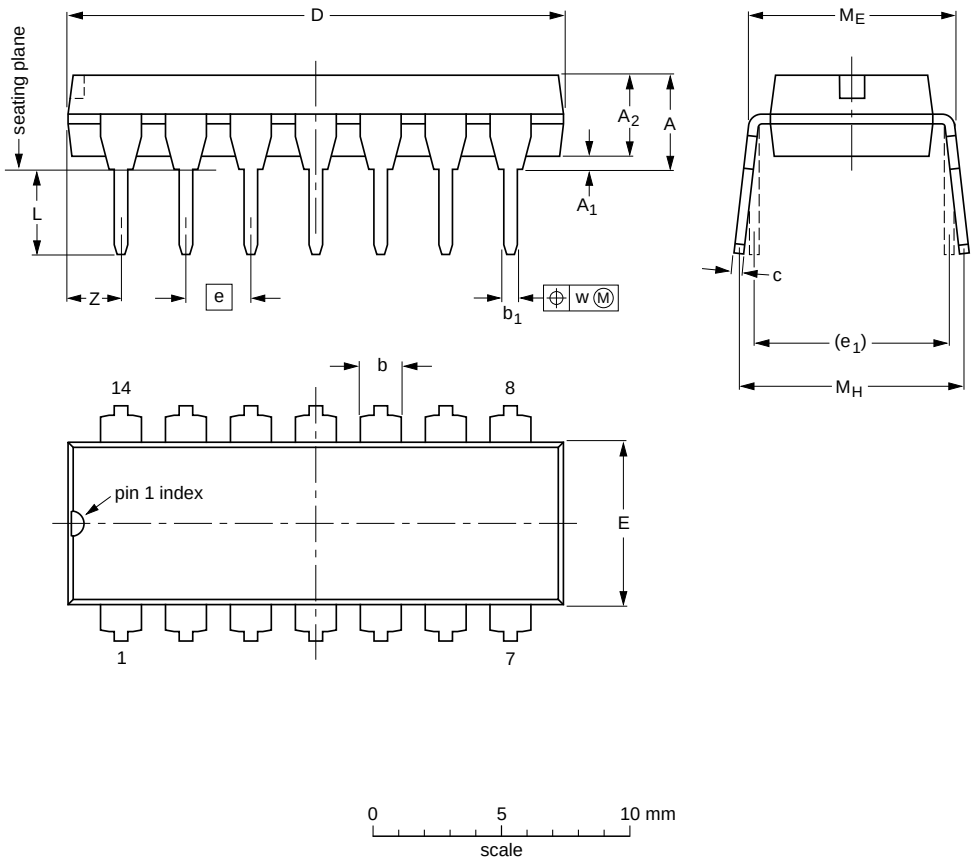
Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

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12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

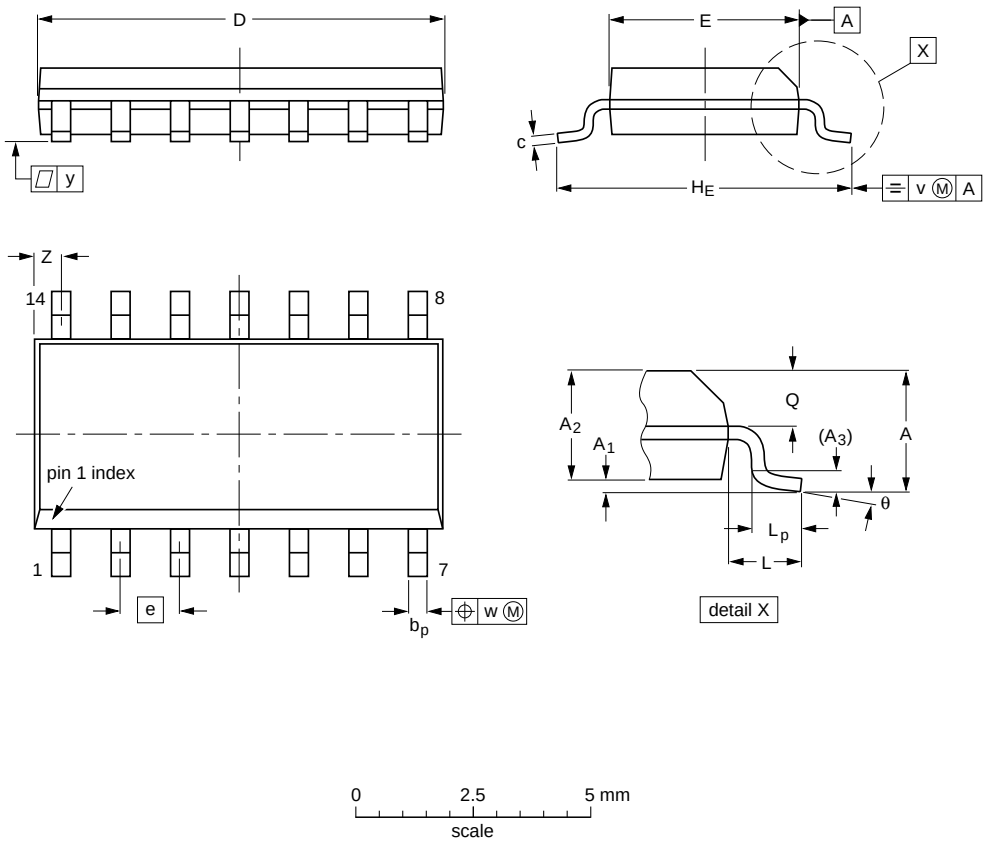
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 9. Package outline SOT27-1 (DIP14)

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SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

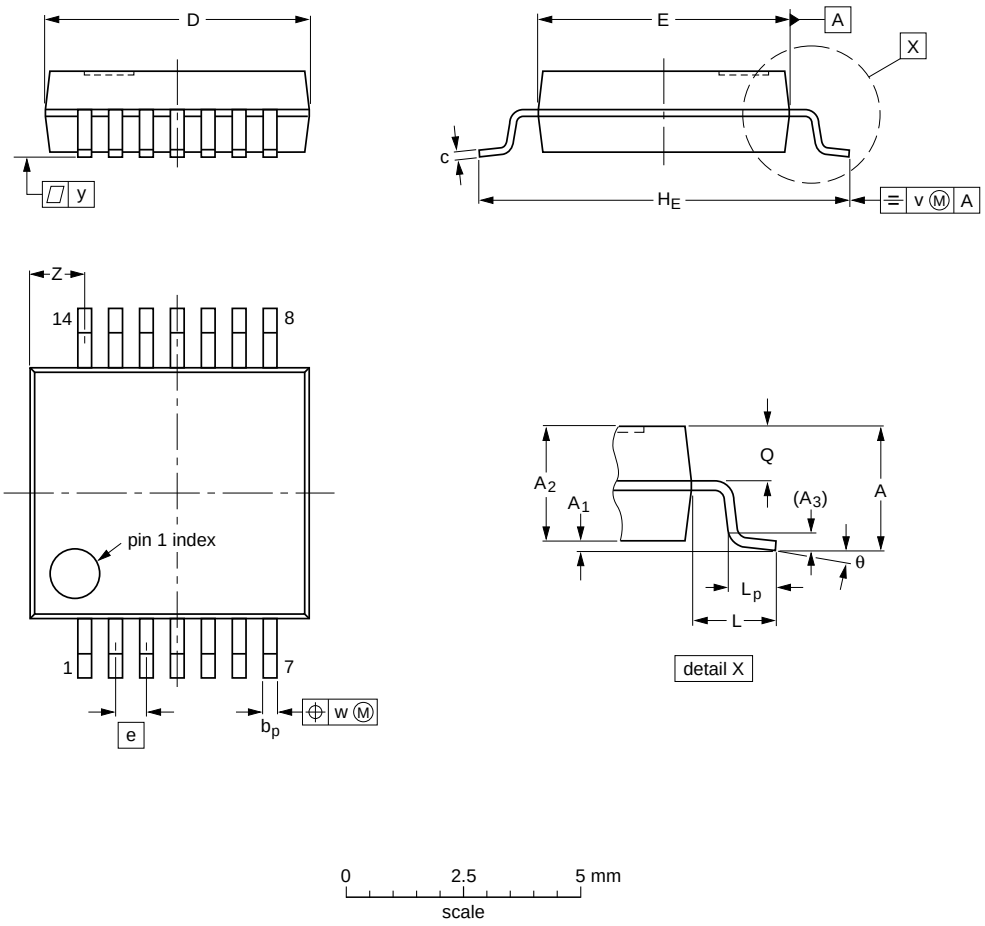
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

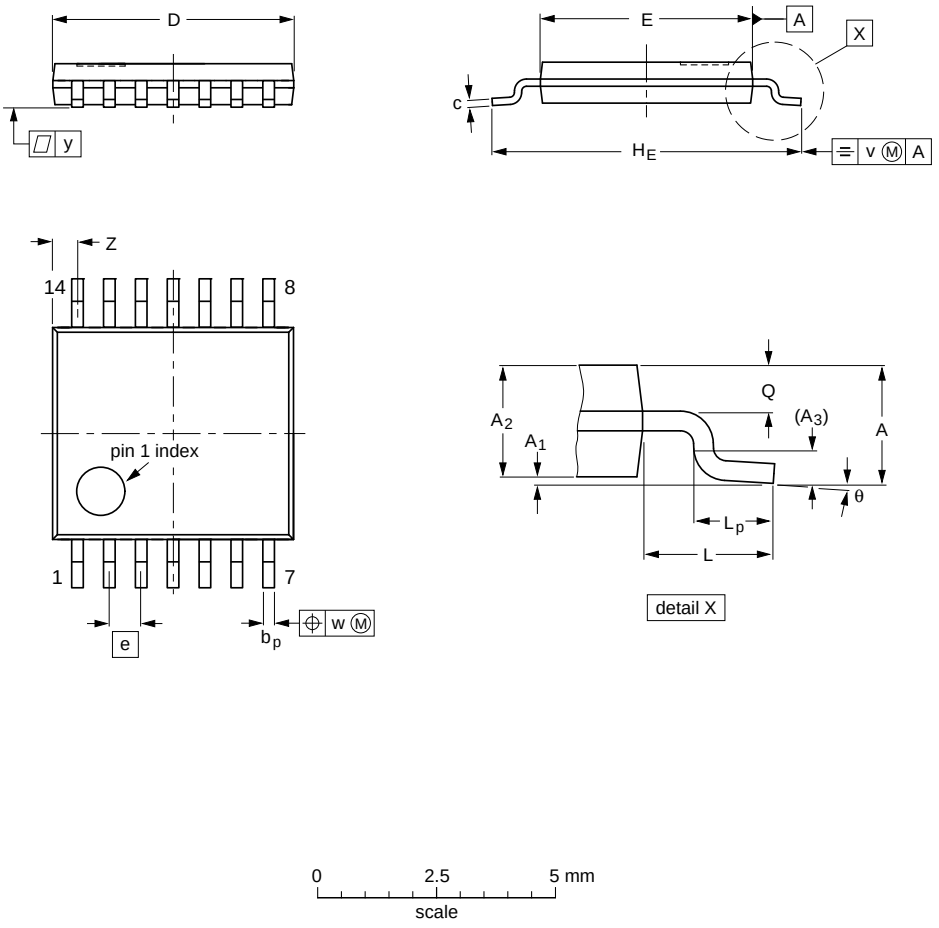
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

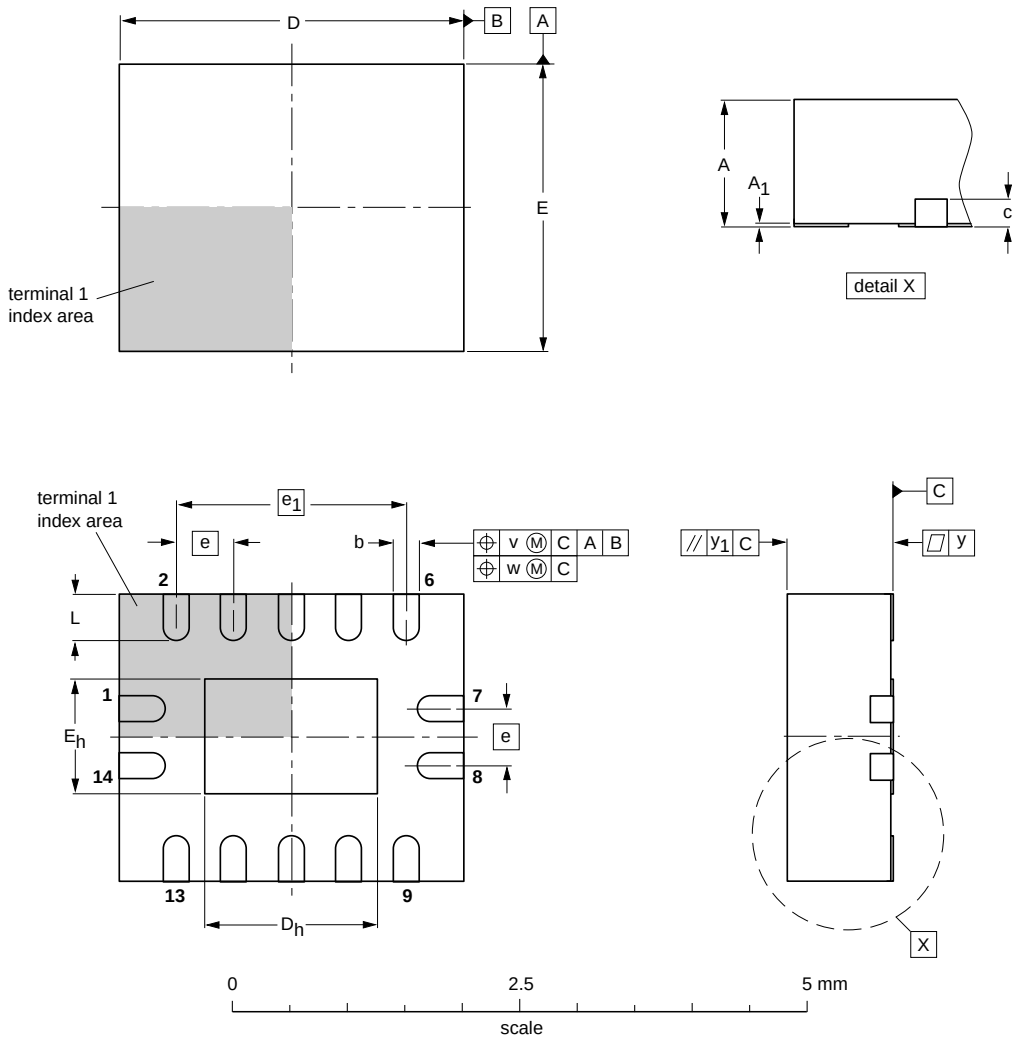
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	BipolarCMOS
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT125 v.6	20111103	Product data sheet	-	74ABT125 v.5
Modifications:	• Legal pages updated			
74ABT125 v.5	20101124	Product data sheet	-	74ABT125 v.4
74ABT125 v.4	20100427	Product data sheet	-	74ABT125 v.3
74ABT125 v.3	20080429	Product data sheet	-	74ABT125 v.2
74ABT125 v.2	19980116	Product specification	-	74ABT125 v.1
74ABT125 v.1	19960305	-	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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